Configuring Multiple FLEX 8000 Devices

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Introduction

The architecture of Altera's Flexible Logic Element MatriX (FLEX) devices supports several methods for configuring multiple FLEX 8000 devices in a single system. You can configure FLEX 8000 devices either individually or together in a parallel or serial fashion.

This application note describes how to create configuration circuits for multiple FLEX 8000 devices. It provides sample schematics, required configuration option bit and configuration pin settings, programming file information, and, where appropriate, timing information. The following topics are discussed:

- ❏ Choosing a configuration circuit
- ❏ Common features in multi-device configuration circuits
- ❏ Multi-Device Sequential Active Serial (MD-SAS) configuration
- ❏ Multi-Device Active Serial Bit-Slice (MD-ASB) configuration
- ❏ Multi-Device Passive Serial Bit-Slice (MD-PSB) configuration
- ❏ Multi-Device Passive Parallel Synchronous (MD-PPS) configuration
- ❏ Multi-Device Passive Parallel Asynchronous (MD-PPA) configuration
- ❏ Multi-Device Active Parallel Hybrid (MD-APH) configuration

This application note must be used together with *Application Note 33 (Configuring FLEX 8000 Devices)*, which provides detailed information on FLEX 8000 device operating modes, data-space sizes, in-circuit reconfiguration, configuration option bits, configuration pins, programming file generation, and single-device configuration. Refer also to the *FLEX 8000 Programmable Logic Device Family* and *Configuration EPROMs for FLEX Devices* data sheets for additional details on device architecture.

Choosing a Configuration Circuit

The best type of configuration for a particular system depends on a variety of factors, including the existing resources in the system, the number of devices to be configured, the desired configuration time, reconfiguration requirements, and the need to periodically load new configuration data. Table 1 summarizes the characteristics of the multi-device configuration circuits supported by the FLEX 8000 architecture.

Table 1. FLEX 8000 Configuration Schemes

Configuration Circuit	Intelligent Host Required	Auto-Reconfiguration Available	Concurrent Device Configuration	Simultaneous Device Initialization	Configuration Data Location	Max. Devices Configured	Programming File(s)
Multi-Device Sequential Active Serial (MD-SAS)	No	No	No	No	Configuration EPROM(s)	Unlimited	Programmer Object File (**.pof**)
Multi-Device Active Serial Bit-Slice (MD-ASB)	No	Yes	Yes	Yes	Parallel EPROM	8	Hexadecimal (Intel-format) File (**.hex**)
Multi-Device Passive Serial Bit-Slice (MD-PSB)	Yes	No	Yes	Yes	Data file(s)	8 per data file	Tabular Text File (**.ttf**)
Multi-Device Passive Parallel Synchronous (MD-PPS)	Yes	No	Yes	Yes	Data files	Unlimited *Note (1)*	Tabular Text File (**.ttf**)
Multi-Device Passive Parallel Asynchronous (MD-PPA)	Yes	No	Yes	Yes	Data files	Unlimited *Note (2)*	Tabular Text File (**.ttf**)
Multi-Device Active Parallel Hybrid (MD-APH)	No	No	No	No	Parallel EPROM	9	Hexadecimal (Intel-format) File (**.hex**)

Notes:
(1) One FLEX 8000 device can be configured for each unique DCLK signal generated by an intelligent host.
(2) One FLEX 8000 device can be configured for each uniquely decodable address.

This application note describes each type of configuration circuit in detail, the configuration scheme used for each device, the connections between devices, and how to generate the configuration data. The term *configuration scheme* refers to the bit pattern of the nSP, mSEL1, and mSEL0 selection bits—and the attendant behavior—of a single, specific FLEX 8000 device. In contrast, the term *configuration circuit* refers to a set of multiple FLEX 8000 devices, the configuration schemes used for each FLEX 8000 device, and the connections between the devices. In a multi-device system, each FLEX 8000 device in the configuration circuit can use a different configuration scheme.

Common Features in Multi-Device Configuration Circuits

Multi-device configuration circuits have several common characteristics. The following features have similar purposes in each configuration circuit:

- ❏ Configuration Clock frequency
- ❏ nCONFIG pin
- ❏ nSTATUS pin
- ❏ CONF_DONE pin

For more detailed information on these items, refer to *Application Note 33 (Configuring FLEX 8000 Devices)*.

Configuration Clock Frequency

The Clock source for all active configuration schemes is an internal oscillator in the FLEX 8000 device, which typically operates in the range 2 MHz to 6 MHz. In all passive configuration schemes, an external controller guides the device configuration at a maximum frequency of 2 MHz.

nCONFIG Pin

In most configuration circuits, the nCONFIG input pin on a FLEX 8000 device is connected to V_{CC}. At system power-up, this connection directs the device to immediately start configuration (in an active configuration scheme) or to prepare for immediate configuration (in a passive configuration scheme).

If an application requires a delay in the FLEX 8000 device configuration, the nCONFIG pin must be tied to external logic. A high-to-low transition on nCONFIG resets the FLEX 8000 device, and a subsequent low-to-high transition starts the configuration process.

nSTATUS Pin

In most configuration circuits, the bidirectional nSTATUS pin on a FLEX 8000 device is connected to an intelligent host or to external support logic. If an error occurs during device configuration, this pin is pulled and held low.

CONF_DONE Pin

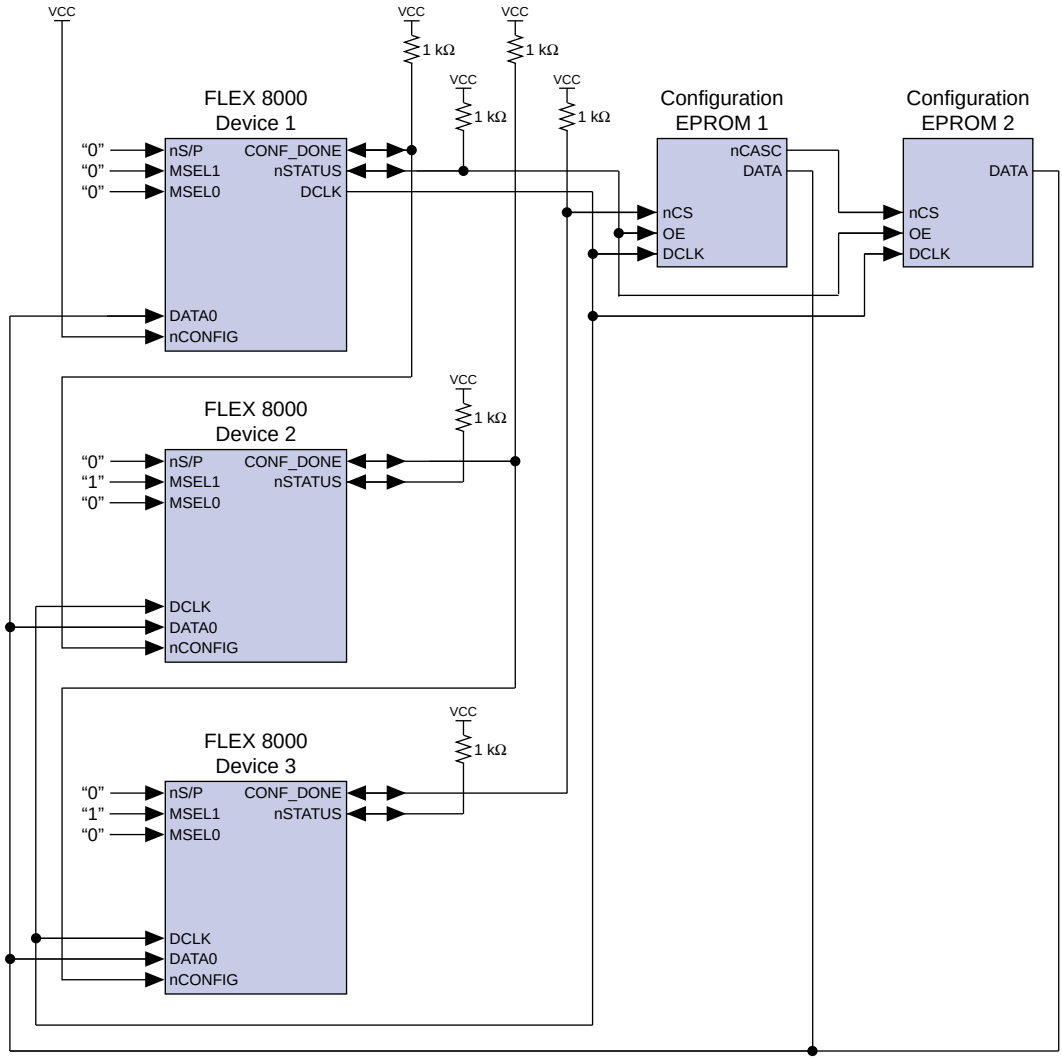
In most configuration circuits, the bidirectional CONF_DONE pins on each FLEX 8000 device are connected to the same net. The FLEX 8000 devices in the circuit hold the CONF_DONE net low until all devices are fully configured, thereby allowing devices of different sizes to be configured and initialized simultaneously. The CONF_DONE net is also connected to the DONE input of the external support logic or an intelligent host to indicate that configuration has been successful.

Multi-Device Sequential Active Serial (MD-SAS) Configuration

In an MD-SAS configuration circuit, the configuration data is stored in one or more Altera serial Configuration EPROMs. The first FLEX 8000 device controls the configuration by generating a DCLK signal that clocks data out from the Configuration EPROMs. The CONF_DONE pin on the first FLEX 8000 device is connected to the nCONFIG pin of the next FLEX 8000 device, and the connection is repeated through the entire configuration circuit. Once the first FLEX 8000 device is fully configured, its CONF_DONE pin is pulled up to V_{CC} via an external pull-up resistor. This low-to-high transition on the nCONFIG input to the next FLEX 8000 device directs it to begin configuration.

Figure 1 shows three FLEX 8000 devices and two Configuration EPROMs in an MD-SAS configuration circuit. By default, each FLEX 8000 device in a project has one dedicated Configuration EPROM. In this example, however, the configuration data for the three FLEX 8000 devices has been combined and programmed into two Configuration EPROMs. In some circuits, you may need more Configuration EPROMs than FLEX 8000 devices to store the configuration data (e.g., three EPC1213 Configuration EPROMs are required to configure two EPF81500 devices). When you combine the programming files for the Configuration EPROMs, the MAX+PLUS II software automatically calculates the minimum number of Configuration EPROMs needed to support a multi-device configuration circuit.

Figure 1. Multi-Device Sequential Active Serial (MD-SAS) Configuration Circuit



The nCS pin on the first Configuration EPROM must be connected to the CONF_DONE output of the last FLEX 8000 device in the circuit to ensure that all Configuration EPROMs are disabled after the last FLEX 8000 device is completely configured. In addition, if the configuration circuit includes more than six devices, the DCLK and DATA0 nets should have external active buffering to maintain the signal integrity. Table 2 summarizes the configuration parameters for MD-SAS configuration circuits.

Table 2. MD-SAS Configuration Parameters

Parameter	Description
Configuration scheme	First FLEX 8000 device: Active Serial (nSP:mSEL1:mSEL0 = 000) Subsequent FLEX 8000 device(s): Passive Serial (nSP:mSEL1:mSEL0 = 010)
Non-default device option & configuration pin settings	For the first FLEX 8000 device only, turn on the *Enable DCLK Output in User Mode* option in the **FLEX 8000 Individual Device Options** dialog box. DCLK is inactive in subsequent FLEX 8000 devices, which use the Passive Serial configuration scheme.
Device configuration/ programming file	Configuration data is stored in one or more POFs, depending on the number of Configuration EPROMs required to configure the FLEX 8000 devices. POFs are generated by combining the SRAM Object Files (**.sof**) from all FLEX 8000 devices in the serial order in which they are configured on the board. Select *.pof (Sequential)* in the *File Format* drop-down list box in the **Combine Programming Files** dialog box when generating POFs for MD-SAS configuration.
Reconfiguration on error	No automatic reconfiguration is available. The nSTATUS pin is connected to V_{CC} separately on each FLEX 8000 device. Each of the nSTATUS nets must be monitored for a high-to-low transition, which indicates that an error has occurred during configuration. The nCONFIG pin on the first FLEX 8000 device must be pulled low and then released to initiate a reconfiguration cycle.

Multi-Device Active Serial Bit-Slice (MD-ASB) Configuration

In an MD-ASB configuration circuit, the configuration data is stored in a parallel EPROM. The EPROM must have a maximum access time of 100 ns. Each bit in the EPROM data word (up to 8 bits wide) configures a different FLEX 8000 device. Data in the EPROM is presented as parallel streams of serial configuration data. A standard byte-wide EPROM can configure up to eight FLEX 8000 devices simultaneously, with each data pin in the EPROM data word connected to the DATA0 pin of the corresponding FLEX 8000 device in the configuration circuit.

Figure 2 shows an MD-ASB circuit in which two FLEX 8000 devices are configured with a parallel EPROM. A support PLD such as the EPM7032 device translates the DCLK signals generated by the first FLEX 8000 device into sequential addresses for the parallel EPROM. This support device must contain an 18-bit counter and other logic to translate nSTATUS into a global Reset signal.

Figure 2. Multi-Device Active Serial Bit-Slice (MD-ASB) Configuration Circuit

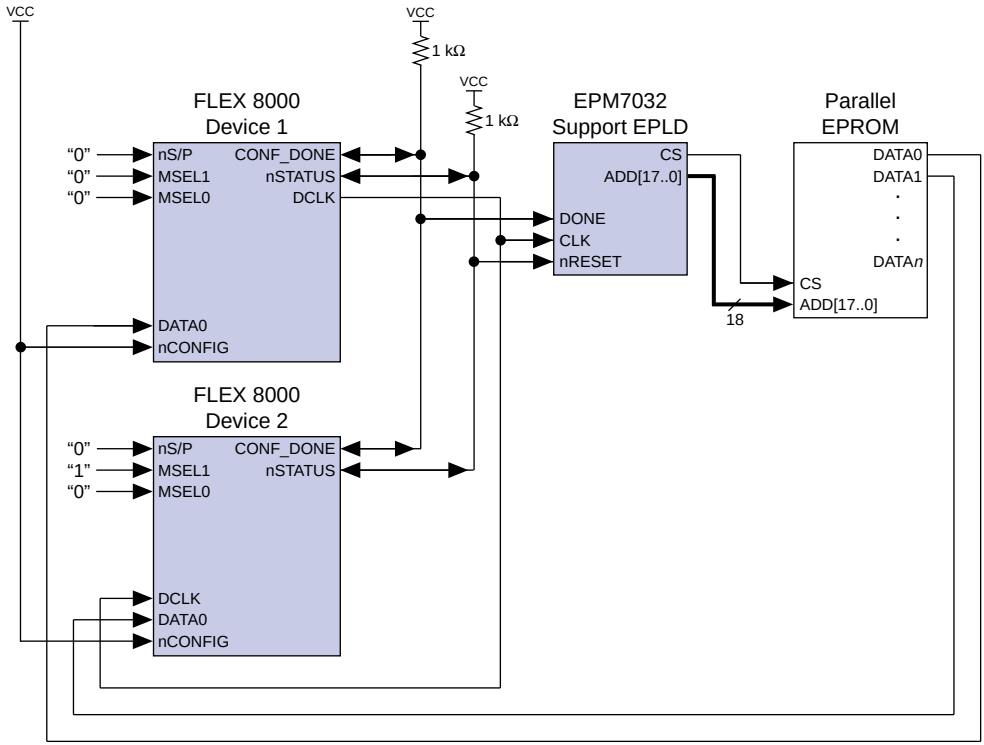


Figure 3 shows an Altera Hardware Description Language (AHDL) Text Design File (**.tdf**) that implements the features required in an EPM7032 support device.

Figure 3. AHDL Text Design File for EPM7032 Support Device (asbpld.tdf)

```
DESIGN IS asbpld
   DEVICE IS EPM7032LC44;

SUBDESIGN asbpld
(
   clk, done, nreset : INPUT;
   cs, add[17..0]    : OUTPUT;
)

VARIABLE
   count[17..0]      : DFF;
   atri[17..0]       : TRI;

BEGIN
   add[]        = atri[];
   atri[]       = count[];
   atri[].oe    = global(!done);
   cs           = !done;

   count[].clk  = global(clk);
   count[].clrn = global(nreset);
   count[].d    = count[].q + 1;

END;
```

Table 3 summarizes the configuration parameters for MD-ASB configuration circuits.

Table 3. MD-ASB Configuration Parameters

Parameter	Description
Configuration scheme	First FLEX 8000 device: Active Serial (nSP:mSEL1:mSEL0 = 000) Subsequent FLEX 8000 device(s): Passive Serial (nSP:mSEL1:mSEL0 = 010)
Non-default device option & configuration pin settings	For all FLEX 8000 devices, turn on the *Disable Start-Up Time-Out* option in the **FLEX 8000 Device Options** dialog box. For the first FLEX 8000 device, turn on the *Auto-Restart Configuration on Frame Error* option in the **FLEX 8000 Individual Device Options** dialog box.
Device configuration/ programming file	Configuration data is stored in a single Hex File, generated by combining the SOFs from all FLEX 8000 devices in the parallel order in which they are configured on the board. Select *.hex (Bit-Slice)* in the *File Format* drop-down list box in the **Combine Programming Files** dialog box when generating Hex Files for MD-ASB configuration. The first file listed in the **Combine Programming Files** dialog box corresponds to DATA0 on the EPROM, the second corresponds to DATA1, and so on.
Reconfiguration on error	The circuit in Figure 2 supports automatic reconfiguration on error. A FLEX 8000 device drives a high-low-high pulse on the nSTATUS signal whenever a configuration error (e.g., bad data) or an operation error (e.g., V_{CC} failure) occurs. This pulse resets the counter in the EPM7032 support PLD and restarts the configuration process.

Multi-Device Passive Serial Bit-Slice (MD-PSB) Configuration

In the MD-PSB configuration circuit, the configuration data is typically stored in a data file and presented to the FLEX 8000 devices by an intelligent host. The data in the configuration file incorporates parallel streams of serial configuration data. Each bit in the 8-bit-wide configuration file provides configuration data to the DATA0 pin of a separate FLEX 8000 device in the configuration circuit. After it has presented a data word on the data bus, the intelligent host sends a DCLK pulse to all FLEX 8000 devices, instructing them to latch the data.

Figure 4 shows two FLEX 8000 devices that are configured by an intelligent host in an MD-PSB configuration circuit.

Figure 4. Multi-Device Passive Serial Bit-Slice (MD-PSB) Configuration Circuit

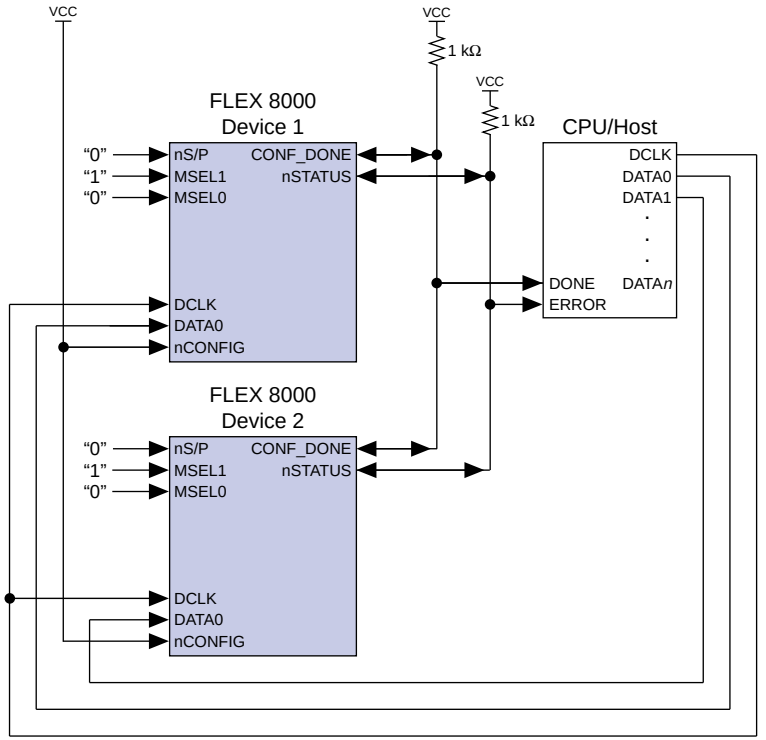


Figure 5 shows the sequence of control signals that the intelligent host must generate to correctly implement the circuit. A single configuration file can provide the data to simultaneously configure up to eight FLEX 8000 devices; multiple files can be used to extend an MD-PSB configuration circuit without limit.

Figure 5. Multi-Device Passive Serial Bit-Slice (MD-PSB) Configuration Waveforms

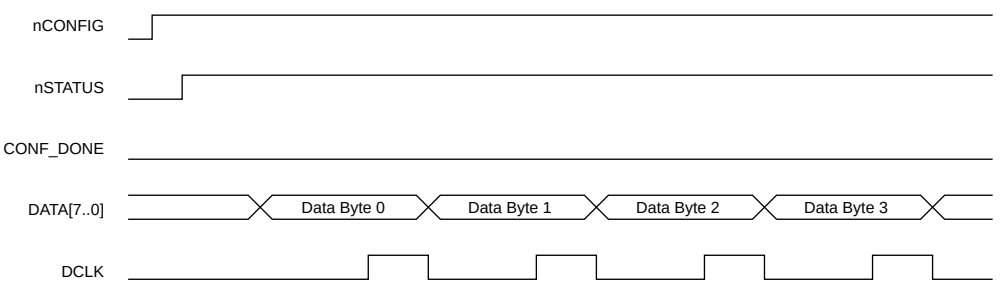


Table 4 summarizes the configuration parameters for MD-PSB configuration circuits.

Table 4. MD-PSB Configuration Parameters

Parameter	Description
Configuration scheme	First FLEX 8000 device: Passive Serial (nSP:mSEL1:mSEL0 = 010) Subsequent FLEX 8000 device(s): Passive Serial (nSP:mSEL1:mSEL0 = 010)
Non-default device option & configuration pin settings	If the FLEX 8000 device uses DATA0 during user mode, you must turn off the *Reserve* option for DATA0 for all FLEX 8000 devices in the **FLEX 8000 Device Options** dialog box. For all FLEX 8000 devices, turn on the *Disable Start-Up Time-Out* option in the **FLEX 8000 Device Options** dialog box.
Device configuration/ programming file	Configuration data is stored in a single TTF, generated by combining the SOFs from all FLEX 8000 devices in the *parallel* order in which they are configured on the board. The first file listed corresponds to the least significant bit (LSB) of the TTF. Select *.ttf (Bit-Slice)* from the *File Format* drop-down list box in the **Combine Programming Files** dialog box when generating TTFs for MS-PSB configuration. A TTF can contain up to eight parallel configuration bit-streams; the data in the file must be converted from ASCII to binary format before being presented to the FLEX 8000 devices during configuration. The Altera Applications BBS provides the **ttf2rbf** conversion utility for this purpose.
Reconfiguration on error	No automatic reconfiguration is available. The circuit shown in Figure 4 shows an input to the intelligent host called ERROR, which must be monitored for a high-to-low transition on the nSTATUS signal. This transition indicates an error during configuration or user-mode operation. The intelligent host must respond by pulling nCONFIG low to initiate a reconfiguration cycle, then releasing it.

Multi-Device Passive Parallel Synchronous (MD-PPS) Configuration

In an MD-PPS configuration circuit, the configuration data is typically stored in data files on a hard disk. An intelligent host presents the data to the FLEX 8000 devices in a parallel format on an 8-bit-wide data bus. Each FLEX 8000 device in the circuit can be configured sequentially, so that each successive device is completely configured before the next device starts configuration. Alternatively, the configuration can be interleaved, with each FLEX 8000 device receiving one data byte in rotation. Each FLEX 8000 device requires a separate DCLK control input from the intelligent host, and must be clocked eight times for each byte at a frequency up to 2 MHz.

Figure 6 shows an MD-PPS configuration circuit in which an intelligent host configures two FLEX 8000 devices. This configuration circuit can be extended to include one FLEX 8000 device for each unique DCLK signal generated by the intelligent host.

Figure 6. Multi-Device Passive Parallel Synchronous (MD-PPS) Configuration Circuit

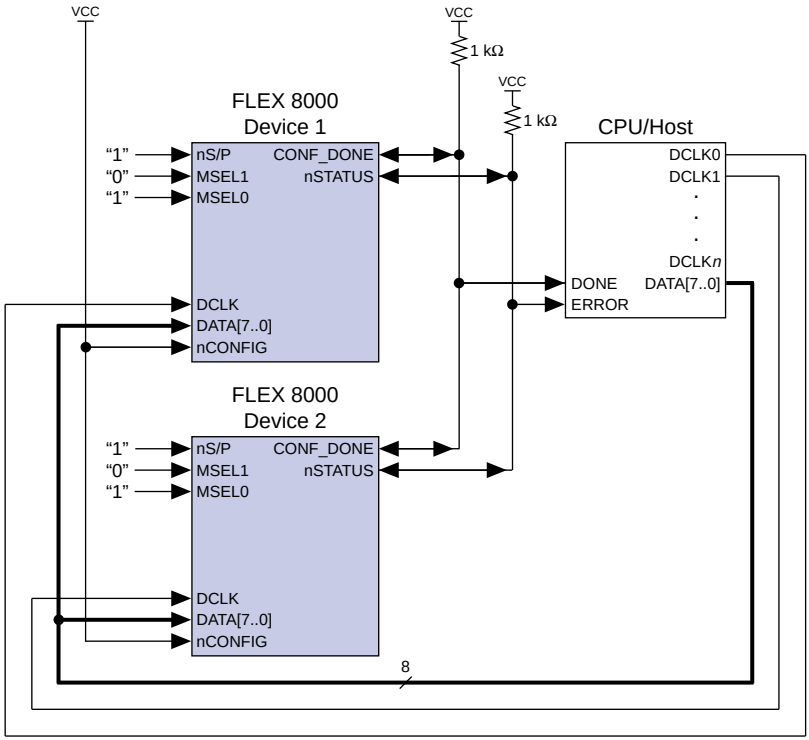


Figure 7 shows the sequence of control signals necessary for both interleaved and non-interleaved MD-PPS configuration.

Figure 7. Multi-Device Passive Parallel Synchronous (MD-PPS) Configuration Waveforms

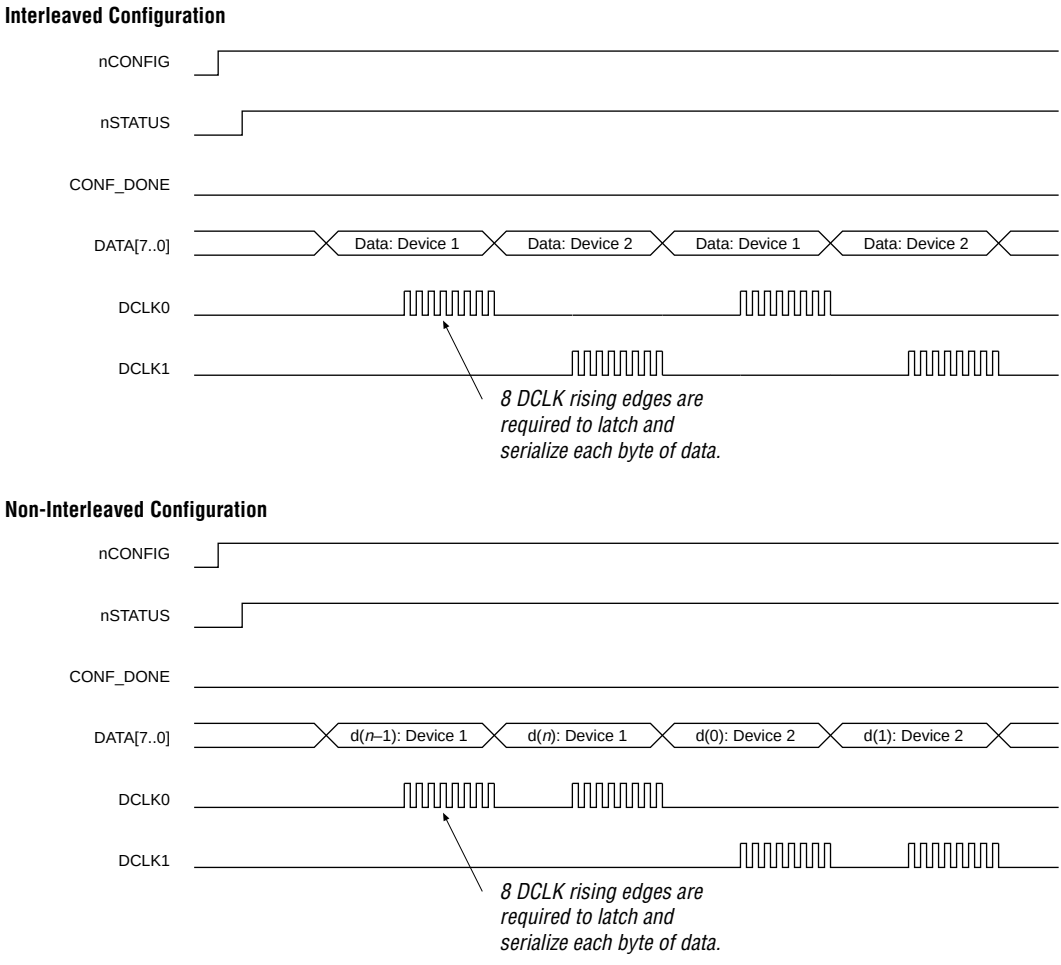


Table 5 summarizes the configuration parameters for MD-PPS configuration circuits.

Table 5. MD-PPS Configuration Parameters

Parameter	Description
Configuration scheme	First FLEX 8000 device: Passive Parallel Synchronous (nSP:mSEL1:mSEL0 = 101) Subsequent FLEX 8000 device(s): Passive Parallel Synchronous (nSP:mSEL1:mSEL0 = 101)
Non-default device option & configuration pin settings	If the FLEX 8000 device uses the data bus during user mode, you must turn off the *Reserve* option for DATA[0..7] for all FLEX 8000 devices in the **FLEX 8000 Device Options** dialog box. For all FLEX 8000 devices, turn on the *Disable Start-Up Time-Out* option in the **FLEX 8000 Device Options** dialog box.
Device configuration/ programming file	Configuration data is stored in a separate TTF for each device. Select *.ttf (Sequential)* from the *File Format* drop-down list box in the **Combine Programming Files** dialog box when generating TTFs for MD-PPS configuration. The TTF data must be converted from ASCII to binary format before being presented to the FLEX 8000 devices during configuration. The Altera Applications BBS provides the **ttf2rbf** conversion utility for this purpose.
Reconfiguration on error	No automatic reconfiguration is available. The circuit in Figure 6 shows an input to the intelligent host called ERROR, which must be monitored for a high-to-low transition on the nSTATUS signal. This transition indicates an error during configuration or user-mode operation. The intelligent host must respond by pulling nCONFIG low to initiate a reconfiguration cycle, then releasing it.

Multi-Device Passive Parallel Asynchronous (MD-PPA) Configuration

In the MD-PPA configuration circuit, the configuration data is typically stored in data files on hard disk. An intelligent host presents the data to the FLEX 8000 devices in a parallel format on an 8-bit-wide data bus. Each FLEX 8000 device in the circuit can be configured sequentially, so that each successive device is completely configured before the next device starts configuration. Alternatively, the configuration can be interleaved, with each FLEX 8000 device receiving one data byte in rotation. If the data bus is very fast, you may wish to use the interleaving method to take advantage of the FLEX 8000 device's 4-µs (250-kHz) minimum configuration time per byte. Otherwise, sequential configuration may be more appropriate.

Each FLEX 8000 device is uniquely addressed by a decoder PLD. When the intelligent host is ready to present a data byte to a FLEX 8000 device, the host generates the corresponding address and the decoder PLD selects the correct FLEX 8000 device using the nCS pin. The intelligent host then provides a high-low-high pulse on nWS, which directs the selected FLEX 8000 device to latch the data. A high-low-high pulse on nRS directs the addressed FLEX 8000 device to present the RDYnBUSY signal on the DATA7 pin, which must be monitored to determine when the FLEX 8000 device is ready to receive another byte of data. The DATA7 pin on the intelligent host must be tri-stated during the monitoring process.

Figure 8 shows two FLEX 8000 devices, an intelligent host, and a decoder PLD in an MD-PPA configuration circuit. This configuration circuit can be extended to include one FLEX 8000 device for each uniquely decodable address, with no upper limit to the number of devices.

Figure 8. Multi-Device Passive Parallel Asynchronous (MD-PPA) Configuration Circuit

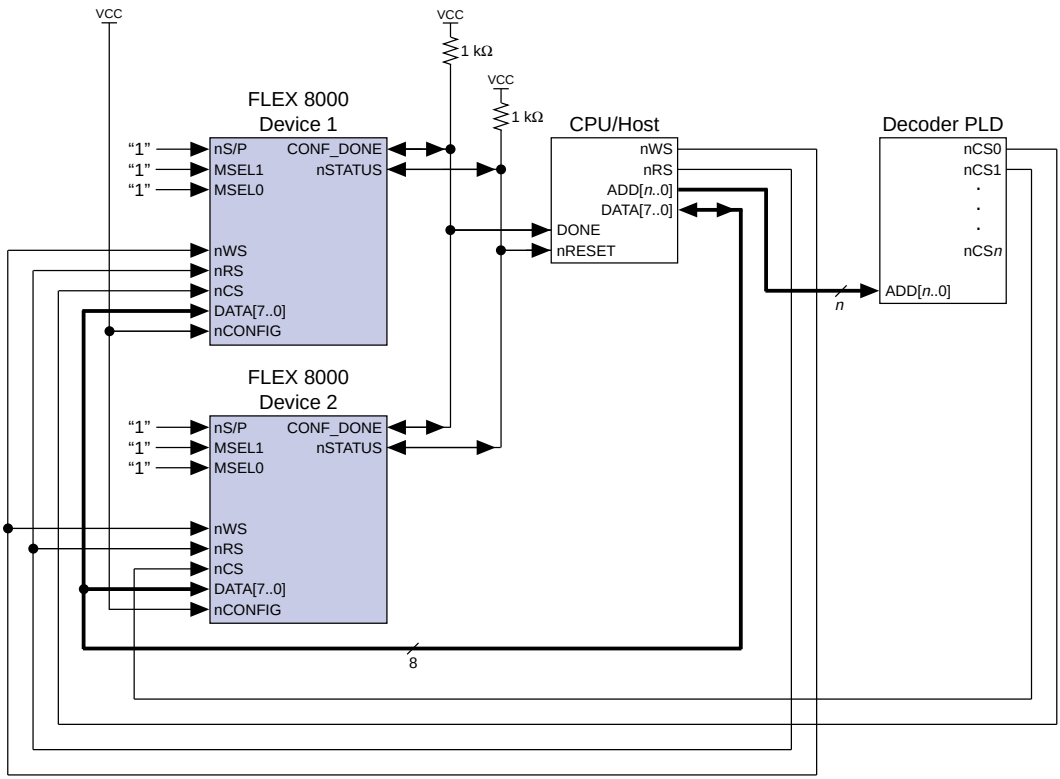


Figure 9 shows the sequence of control signals necessary for a non-interleaved MD-PPA configuration circuit that uses the DATA7 pin for status-checking.

Figure 9. Multi-Device Passive Parallel Asynchronous (MD-PPA) Configuration Waveforms

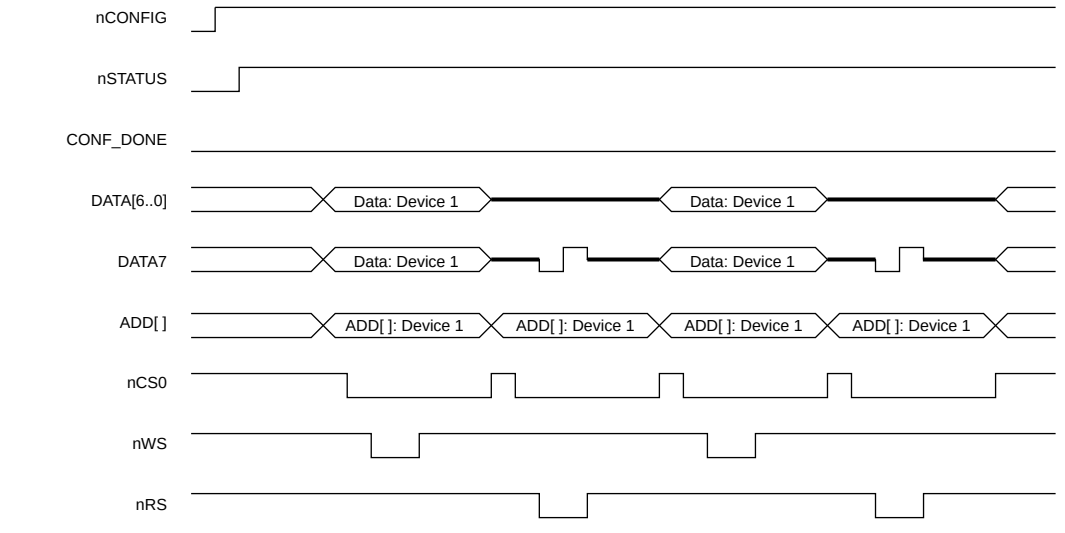


Table 6 summarizes the configuration parameters for MD-PPA configuration circuits.

Table 6. MD-PPA Configuration Parameters

Parameter	Description
Configuration scheme	First FLEX 8000 device: Passive Parallel Asynchronous (nSP:mSEL1:mSEL0 = 111) Subsequent FLEX 8000 device(s): Passive Parallel Asynchronous (nSP:mSEL1:mSEL0 = 111)
Non-default device option & configuration pin settings	If the FLEX 8000 device uses the data bus during user mode, you must turn off the *Reserve* option for DATA[0..7] for all FLEX 8000 devices in the **FLEX 8000 Device Options** dialog box. For all FLEX 8000 devices, turn on the *Disable Start-Up Time-Out* option in the **FLEX 8000 Device Options** dialog box.
Device configuration/ programming file	Configuration data is stored in a TTF for each device. Select *.ttf (Sequential)* from the *File Format* drop-down list box in the **Combine Programming Files** dialog box when generating TTFs for MD-PPA configuration. The TTF data must be converted from ASCII to binary format before being presented to the FLEX 8000 devices during configuration. The Altera Applications BBS provides the **ttf2rbf** conversion utility for this purpose.
Reconfiguration on error	No automatic reconfiguration is available. The circuit in Figure 8 shows an input to the intelligent host called ERROR, which must be monitored for a high-to-low transition on the nSTATUS signal. This transition indicates an error during configuration or user-mode operation. The intelligent host must respond by pulling nCONFIG low to initiate a reconfiguration cycle, then releasing it.

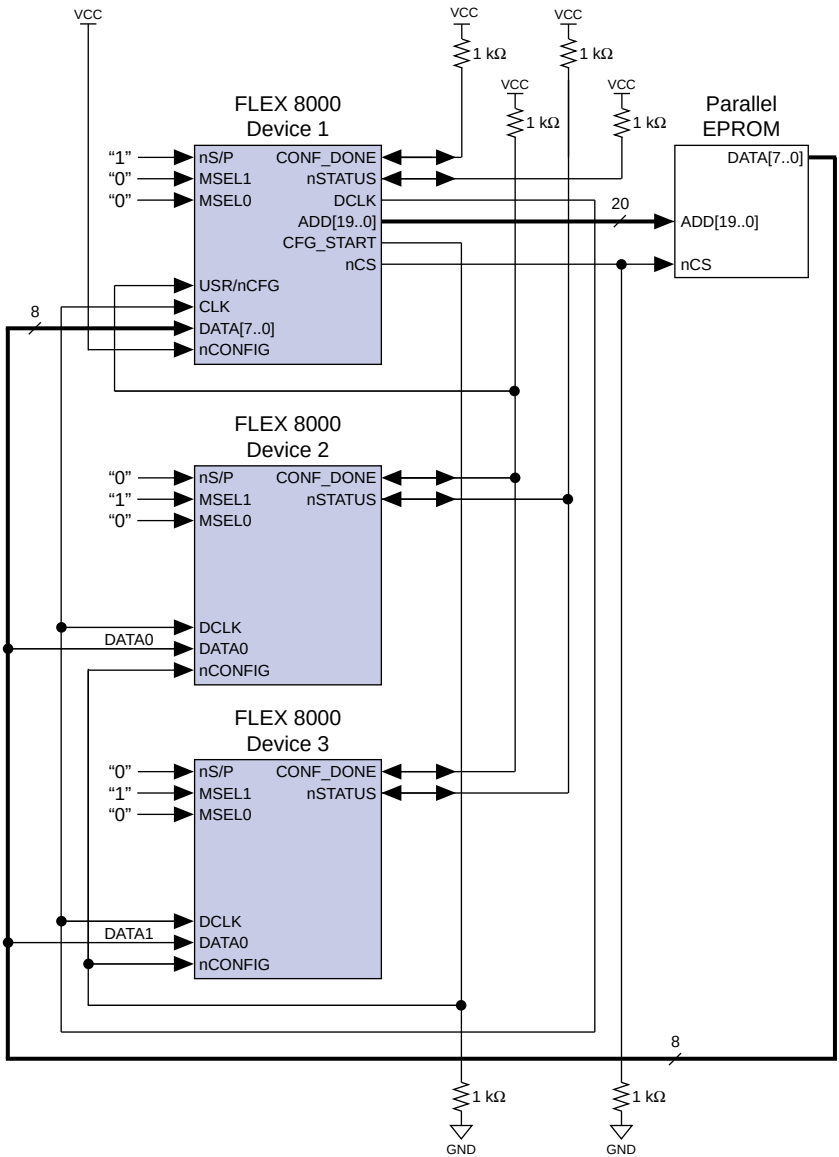
Multi-Device Active Parallel Hybrid (MD-APH) Configuration

In an MD-APH configuration circuit, two configuration data files are stored in a parallel EPROM. The EPROM must have a maximum access time of 100 ns. The first file is used to configure the first FLEX 8000 device in an active parallel up (APU) configuration scheme. The second file consists of serial bit-slice data that can configure up to eight additional FLEX 8000 devices in a passive serial (PS) configuration scheme.

The design file for the first (actively configured) FLEX 8000 device must contain a 20-bit counter and support logic for passively configuring additional FLEX 8000 devices. This logic emulates the address generation used in a single-device APU configuration. The bit-slice data is presented to the passively configured FLEX 8000 devices as parallel streams of serial configuration data. Each bit in the configuration data word (up to eight bits wide) configures a separate FLEX 8000 device. The MD-APH configuration support logic for the first FLEX 8000 device is available from the Altera Applications bulletin board service (BBS) in the self-extracting file **md_aph.exe**.

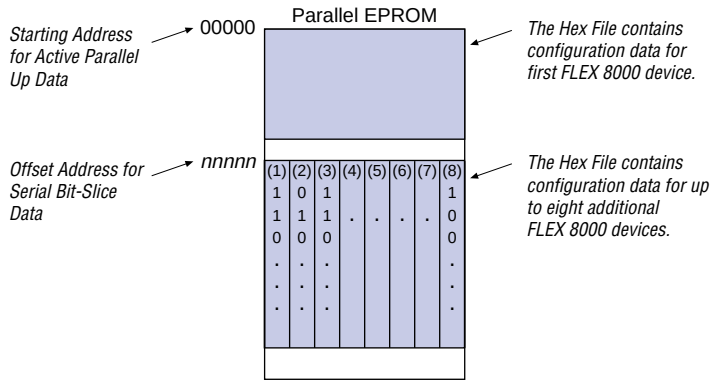
Figure 10 shows an MD-APH circuit in which a parallel EPROM configures three FLEX 8000 devices.

Figure 10. Multi-Device Active Parallel Hybrid (MD-APH) Configuration Circuit



A byte-wide 256-Kbyte EPROM can configure up to nine EPF81188 FLEX 8000 devices. The first 32 Kbytes store the APU data for the first FLEX 8000 device; the next 192 Kbytes contain the bit-slice configuration data for the passively configured devices. See Figure 11. EPROMs of

Figure 11. Multi-Device Active Parallel Hybrid (MD-APH) Data Storage



different sizes can accommodate configuration data for FLEX 8000 devices of different sizes.

The configuration support logic in the first FLEX 8000 device drives the outputs ADD[19..0], CFG_START, and nCS; it uses the inputs CLK and USR/nCFG. The address pins consist of the dual-purpose configuration pins ADD[17..0] and two I/O pins ADD[19..18]. After all passively configured devices are fully configured and have entered user-mode operation, multiplexers in the support logic release the ADD[19..0] address pins on the first FLEX 8000 device for use as normal I/O pins. The CFG_STRT signal synchronizes device configuration by driving the low-high-low pulse on the nCONFIG inputs to the passively configured FLEX 8000 devices.

The CLK input to the first FLEX 8000 device is tied to its DCLK output so that the DCLK signal, which is not available internally, can drive the support logic. The USR/nCFG input on the first FLEX 8000 device is tied to the CONF_DONE net of all passively configured FLEX 8000 devices. Once these devices are fully configured and have released CONF_DONE, the high logic level on the USR/nCFG input to the first FLEX 8000 device turns off the address counter, releasing the ADD[19..0] address pins for use as I/O pins during user-mode operation. This high logic level also causes the first FLEX 8000 device to assert a high logic level on nCS, which disables the EPROM, releases the DATA[7..0] pins on the FLEX 8000 device, and latches CFG_STRT at V_{CC} to prevent erroneous reconfiguration.

The first FLEX 8000 device must enter user mode before the passively configured FLEX 8000 devices so that its support logic can direct their configuration. Therefore, the CONF_DONE signal on the first FLEX 8000 device is not tied to the CONF_DONE net of the other FLEX 8000 devices.

Table 7 summarizes the configuration parameters for MD-APH configuration circuits.

Table 7. MD-APH Configuration Parameters

Parameter	Description
Configuration scheme	First FLEX 8000 device: Active Parallel Up (nSP:mSEL1:mSEL0 = 100) Subsequent FLEX 8000 device(s): Passive Serial (nSP:mSEL1:mSEL0 = 010)
Non-default device option & configuration pin settings	For the first FLEX 8000 device only, turn on the *Enable DCLK Output in User Mode* option in the **FLEX 8000 Individual Device Options** dialog box. For all other FLEX 8000 devices in the circuit, turn on the *Disable Start-Up Time-Out* option in the **FLEX 8000 Individual Device Options** dialog box.
Device configuration/ programming file	Configuration data is stored in two Hex Files. One Hex File is used for the first FLEX 8000 device, with an offset address of 00000. Select *.hex (Sequential)* in the *File Format* drop-down list box in the **Combine Programming Files** dialog box when generating the Hex File for the first FLEX 8000 device. The other Hex File contains bit-slice data, generated by combining the SOFs for all passively configured FLEX 8000 devices in the parallel order in which they are configured on the board. Select *.hex (Bit-Slice)* in the *File Format* drop-down list box in the **Combine Programming Files** dialog box when generating Hex Files for the passively configured devices. The first file in the *Selected Files* list in the **Combine Programming Files** dialog box corresponds to DATA0 on the parallel EPROM (i.e., the first bit of the bit-slice data for the passively configured devices). You must enter a starting address value for this file in the *Address* box that is after the end of the Hex File for the actively configured (first) FLEX 8000 device.
Reconfiguration on error	No automatic reconfiguration is available. The nSTATUS pin on the first FLEX 8000 device is connected to V_{CC} separately from the nSTATUS pins of the passively configured FLEX 8000 devices. Each nSTATUS net must be monitored for a high-to-low transition, which indicates that an error has occurred during configuration. The nCONFIG pin on the first FLEX 8000 device must be pulled low and then released to initiate a reconfiguration cycle.